

Single electron transistor of stack design as ultrasensitive electrometer

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Abstract. We have fabricated and studied the noise characteristics of the stack-junction Single Electron Tunneling (SET) electrometer, in which the island was completely screened from a dielectric substrate. The noise figure of the device was found to be surprisingly low: an equivalent charge noise was less than $8 \times 10^{-6} e/\sqrt{\text{Hz}}$ at the frequency 10 Hz or, in energy units, $30 \hbar$.

Introduction

In the last years the first attempts to define the location of noise sources in metallic Single Electron Tunneling (SET) structures have been done. Noise measurements of SET transistors have detected a trend of the noise increase with the size of an island [1], have shown a correlation of the noise signals of two closely positioned devices [2], have demonstrated that the noise level of the transistor strongly depends on the contact area of its island with a substrate [3]. Recently, it was shown that the transistors of the stack design have the lowest level of the background charge noise measured so far, namely $2.5 \times 10^5 e/\sqrt{\text{Hz}}$ at the frequency 10 Hz [5]. Although the contact area of an island and substrate in these structures was nominally zero, a possible small-area interface could not be ruled out. In this paper we report on the study of an Al SET transistor of “improved” stack geometry which ensured complete screening of the island from the substrate. Our design allows to eliminate completely the influence of the charge noise sources peculiar to a dielectric substrate on the electrometer noise figure.

1 Fabrications and characterizations of the samples

The Al structure (Fig. 1) was fabricated on a Si substrate buffered by a sputtered Al_2O_3 layer 200 nm thick. The traditional shadow evaporation technique and e-beam lithography were used for the structure fabrication process. There were three successive deposition cycles in-situ at three different angles and two oxidation processes in between to form tunnel barriers. In contrast to the previous stacked samples [4, 5], in this device the *entire* island was placed on a bottom electrode of the structure (see Fig. 1). Since the dimensions of the island (nominally 80 nm by 80 nm) were noticeably smaller than the width of the bottom electrode (150 nm), the island was placed with some margins, it was reliably screened from fluctuating charges located in the dielectric substrate. The I–V curves of the structure, having total resistance $R = 1.25 \text{ M}\Omega$ and capacitance of the island $C_\Sigma = C_1 + C_2 + C_g = 270 \text{ aF}$, were measured at $T = 25 \text{ mK}$. These curves showed a finite conductance within the Coulomb blockade region and this pointed out to the existence of a “shunting” channel $R_{\text{shunt}} = 1.9 \text{ M}\Omega$ for current, namely a conducting tunnel barrier between the outer electrodes of the transistor. This fact ensured against possible contact between the island and the substrate, that might occur at the end edge of the bottom conductor. The resistance $R_\Sigma = R_1 + R_2$ of the SET transistor itself (i.e. the tunnel resistance of its two junctions) was evaluated to be

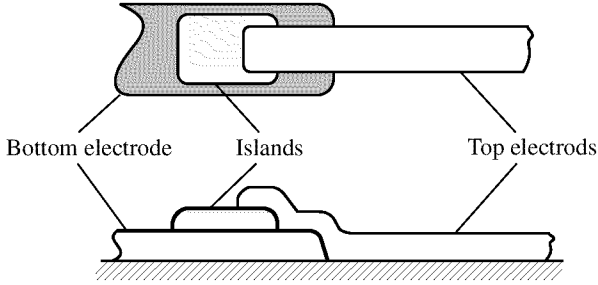


Fig. 1. A geometry of the transistor.

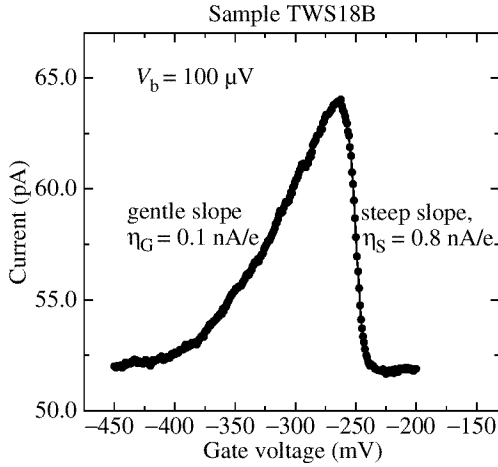


Fig. 2. Modulation curve of the transistor at bias voltage $V_b = 100 \mu\text{V}$.

3.9 MΩ. Expecting a low level of noise in this device and some deterioration of the gain because of shunting channel, we have tried to make the transistor extremely asymmetric in order to get advantage of a steeper slope in the modulation characteristic (see Fig. 2). Fixing of the working point on this slope led to high value of a current-to-charge ratio

$$\eta = \max_{Q_0} \left| \frac{\partial I}{\partial Q_0} \right|_{V=\text{const}}.$$

The values C_1/C_2 and R_2/R_1 , evaluated from experimental data, were in our device as large as 10. The current-to-charge ratio for the steep slopes was in the range $\eta_C \approx 1 - 3 \text{ nA}/e$ depending on voltage across the transistor. These (rather large) values of η had substantially improved the signal-to-noise ratio of our transistor as electrometer.

2 Results and discussion

The transistor clearly exhibited $2e$ -periodic modulation characteristics in the superconducting state and e -periodic modulation in the normal state. (That clearly testified to purity of the island material and its interfaces with the surrounding oxide.) The modulation patterns were surprisingly stable against a drift of the background charge. The output noise of this transistor was measured in the frequency range 0.3–100 Hz at different values of transport current I and in different working points of the modulation characteristic. At low I , the

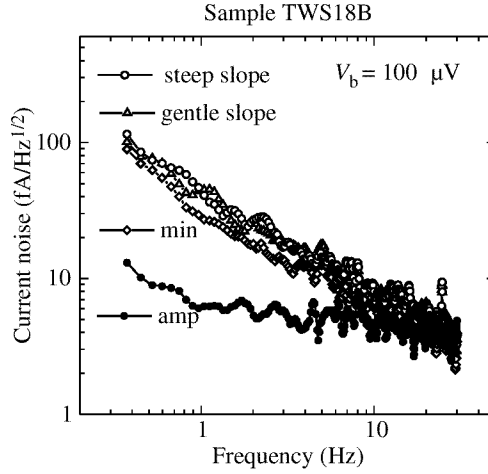


Fig. 3. Noise spectra of the transistor at different points of the modulation curve ($V_b = 100 \mu\text{V}$).

output noise at $f \geq 0.3 \text{ Hz}$ did not show any dependence on the gate voltage (see Fig. 3). This indicated that the charge noise at $I \sim 10 \text{ pA}$ was very small. Thus the noise spectra in the points of the minimum, the gentle and steep slopes of the modulation curve had nearly the same level, which was presumably slightly less than the noise floor of the measuring setup (see the curve marked as *amp* in Fig. 3). The own noise of the preamplifier at 10 Hz was about $5.0 \times 10^{-15} \text{ A}/\sqrt{\text{Hz}}$. The additional shot noise of the shunting junction, due to a current flowing through it, was estimated to be $\delta I = \sqrt{2eI} \approx 4.0 \times 10^{-15} \text{ A}/\sqrt{\text{Hz}}$. Hence, the level of the background charge noise at 10 Hz expressed in current units was less than $6.5 \times 10^{-15} \text{ A}/\sqrt{\text{Hz}}$. The noise figure expressed as an equivalent charge noise δQ_{0x} of the device was found to be less than $8 \times 10^{-6} e/\sqrt{\text{Hz}}$ at 10 Hz or, in energy units,

$$\epsilon = \frac{(\delta Q_{0x})^2}{2C_\Sigma \Delta f} = \frac{S_I}{2C_\Sigma} \approx 30 \hbar$$

To our knowledge, this is the best noise figure of a SET electrometer measured so far. The fundamental noise floor was estimated as $2 \times 10^{-6} e/\sqrt{\text{Hz}}$ [3] or $\epsilon \sim 3 \hbar$. At frequency $f \approx 20 \text{ Hz}$ all noise curves, presented in Fig. 3, have the same level $\delta I \approx 5.0 \times 10^{-15} \text{ A}/\sqrt{\text{Hz}}$ and we can suggest that noise of the electrometer approached the fundamental noise floor set by stochastic tunneling events. Such delicate regime of the electrometer operation ($I \sim 10 \text{ pA}$) demonstrates that contribution of the oxide tunnel barriers to the low-frequency noise can be very small. Therefore, this indicates conclusively that the main sources of the background charge fluctuations in metallic SET devices are located in dielectric substrates and the influence of these sources on the performance of SET devices can be considerably eliminated by screening of the islands from the substrate. The stack geometry of our devices shows one of the ways how to solve the problem of the background charge fluctuations.

Acknowledgements

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